ABSTRACT

More complete charge transfer is achieved in a CMOS or CCD imager by reducing the spacing in the gaps between gates in each pixel cell, and/or by providing a lightly doped region between adjacent gates in each pixel cell, and particularly at least between the charge collecting gate and the gate downstream to the charge collecting gate. To reduce the gaps between gates, an insulator cap with spacers on its sidewalls is formed for each gate over a conductive layer. The gates are then etched from the conductive layer using the insulator caps and spacers as hard masks, enabling the gates to be formed significantly closer together than previously possible, which, in turn increases charge transfer efficiency. By providing a lightly doped region on between adjacent gates, a more complete charge transfer is effected from the charge collecting gate .